

Notice of Allowability

Application No.

10/731,608

Examiner

Ernest F. Karlsen

Applicant(s)

KIM ET AL.

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the filing of 09 December 2003.
2. ☒ The allowed claim(s) is/are 1-13.
3. ☒ The drawings filed on 09 December 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

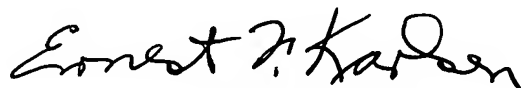
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____



ERNEST KARLSEN
PRIMARY EXAMINER

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: No reference was found anticipating or a combination of references found making obvious an apparatus for controlling delay time in a semiconductor comprising, a test mode delay section outputting control signals in response to a pulse signal, a test delay section outputting a delayed signal delayed for a time dependent on the control signals wherein the delay time to outputting an input signal as an output signal is controlled by the control signals, the control signals being sequentially enabled by the pulse signal and after an (N-1)th control signal is enabled Nth and (N+1)th control signals are alternately enabled every time the pulse signal is toggled and no reference was found anticipating or a combination of references found making obvious a method of controlling a delay time of a signal in a semiconductor device comprising, applying a test mode pulse signal, generating test mode selection signals synchronized with the falling edges of the test mode pulse signal, regenerating a (N-1)th test mode selection signal after a Nth test mode selection signal is generated and repeating the regenerating step wherein an input signal inputted to the semiconductor device is delayed by a predetermined time to be outputted as an output signal only when first to the (N-1)th test mode selection signals are enabled, and the delayed times are different from each other according to the first to the (N-1)th test mode selection signals.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Art Unit: 2829

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Examiner's Comment

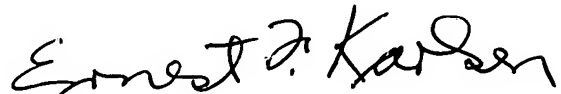
Claims 1-13 are allowed.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugamori, Yoshida, Koyama and Reichle et al are cited to show prior art apparatus and methods for controlling delay time in semiconductor devices.

Any inquiry concerning this communication should be directed to Ernest F. Karlsen at telephone number 571-272-1961.

Ernest F. Karlsen

September 21, 2004

A handwritten signature in black ink that reads "Ernest F. Karlsen". The signature is written in a cursive, flowing style.

**ERNEST KARLSEN
PRIMARY EXAMINER**